Amendments to the Specification

Please replace the paragraph starting on page 8, line 12 with the following:

Fig. 2 is an exemplary block diagram of an integrated circuit 10 that incorporates an embodiment of the invention. A memory cell array 30 of memory cells is preferably arranged in rows and columns, or optionally multiple layers of arrays. Each memory cell in the array 30 can be individually addressed by the use of circuitry in row decoder 34 and column decoder 32. In this embodiment, the row decoder 34 is coupled to a voltage source 36 that is used to apply a range of voltages during programming, reading and non-access of the memory cells. The voltage source 36 may have one or more outputs (shown as signal B 44). Preferably, one output would be used to provide a programming voltage and another output used to provide a read voltage. Alternatively, a programmable voltage source such as a digital to analog converter (DAC) can be used. The voltage source 36 is connected (shown as signal A 42) to control circuitry 40 that also controls the row decoder 34, column decoder 32 and sense circuitry 38. The sense circuitry 38 receives a signal (shown as signal C 46) from the column decoder 32 that detects at least one particular value of an electrical parameter of a selected memory cell from the memory cell array 30. The sense circuitry 38 sends a signal (shown as signal D 48) back to the control circuitry 40 upon detecting a predetermined value.

Please replace the paragraph beginning on page 10, line 3 with the following:

Fig. 3 is an exemplary simplified schematic of a first embodiment 50 of the invention that incorporates the continuous feedback method. A 2 x 2 memory array includes four memory cells 56 that include a control element 54 and a state-change device 52 connected in series. The memory cells 56 are connected to row and column lines used for selection of an individual cell. In this example, the row and column circuitry has been omitted and the non-selected row 64 and the non-selected column 60 are shown as connected to a virtual ground 68. The virtual ground 68 is preferably implemented as a grounded transistor. A voltage

source 70 is connected (using Signal B) to an optional voltage buffer 66 to drive the selected row 62. Voltage source 70 has at least two voltage sources 82, 84 to create program voltage 22 and read voltage 24. The output of voltage source 70 is preferably set by control circuitry 40 using a switch 71 (using Signal A). During programming, the voltage source 70 is set to the program voltage 22 (see Fig. 1) and this voltage is applied across control element 54 and state-change device 52 of the selected memory cell 56. The control circuitry 40 is preferably connected to a digital to analog converter (DAC) 80 with digital inputs 78 (shown as inputs A and B) to select a predetermined voltage output (shown as O) that represents the desired state to be programmed into the state-change device 52. The DAC voltage output is applied to the positive input of an op-amp 76. When the N-FET 72 is off, the positive input of the op-amp 76 is higher than the negative input, the output of the op-amp 76 goes high causing an N-FET 72 to turn on to allow current to flow through sense resistor 74. Because the resistance of the state-change device is high when not programmed the current through a sense resistor 74 is low resulting in a voltage less than the output of the DAC 80. This resistor voltage is applied to the negative input of the op-amp 76. As the state-change device 52 is programmed, the current through the device will increase as its internal resistance is lowered due to the programming process. This increase in current will increase the voltage across sense resistor 74 until the negative input of the op-amp 76 is greater than the output of the DAC 80 connected to the positive input of the op-amp 76. When the negative input is greater than the positive input, the output of the opamp will go low shutting off the current flow through the state-change device 52. The output of the op-amp 76 is sent to the control circuitry 40 (using signal D) to allow it to detect the end of programming and to change the output of the voltage source to a different level such as read voltage 24 or another value such as ground.

Please replace the paragraph starting on page 12, line 4 with the following:

Fig. 5 is an exemplary flow chart of the programming process used by the control circuitry used to change the state of the state-change device in the first embodiment. The control circuitry logic can be implemented in several ways. It can be fixed logic, programmable logic, a programmable processor executing control codes stored in computer executable memory, or a state machine as a few examples. The control circuitry 40 also optionally communicates with other circuitry on or outside of IC 10. In step 100, a state-change element is selected by the control circuitry using the row and column decoders. In step 102, a first voltage equal to the programming voltage is applied to the selected state-change element. In step 104, a value of an electrical parameter, such as current, voltage, resistance, conductance, capacitance, inductance, or impedance of the selected state-change device is detected. In step 106, the detected value of the electrical parameter is compared to a predetermined value assigned by the control circuitry. If the predetermined value is not reached as in step 108, then step 106 is repeated. If the predetermined value is reached, then the control circuitry applies a second voltage, preferably the read voltage to the selected state-change device as in step 110. Optionally in step 112, the control circuitry can verify that the state-change device has been properly programmed by adjusting the predetermined value to another value used during reading of the device, e.g. changing from Iw1 to Ir2, Iw2 to Ir3 as shown in Fig. 1.

Please replace the paragraph starting on page 13 line 8 with the following:

In this second embodiment 51, the control circuitry 40 generates Signal A'. Signal A' is a digital pulse train of one or more bits (shown as bits A and B) that selects the voltage applied by a voltage source digital to analog converter (DAC) 84 and buffer 66 to the selected memory cell 56. The control circuitry 40 also sends a digital code of one or more bits to the input 78 (shown as inputs A and B) of DAC 80 to select a voltage level (shown as output O) that is compared to the converted current (by sense resistor 74) seen through the selected state-change device 52. The converted voltage seen across sense resistor 74 is applied to the input (shown as input I) of a set of fixed comparators or preferably an analog to

digital converter (ADC) 92. The outputs 88 (shown as outputs X and Y) of the ADC 92 are coupled to the control circuitry 40 for determining that the proper state has been reached during programming of the selected state-change device 52. Op-amp 76 is still used to enable and disable programming of the selected state-change device 52 by controlling the N-FET 72. Signal D' is shown as an inverted signal of op-amp 76 and is coupled to the control circuitry 40 so it can be monitored during the programming cycle. Signal C' is a representation of the current seen through the selected state-change device 52 during the programming process. Signal B' represents the output of the voltage source DAC 84.